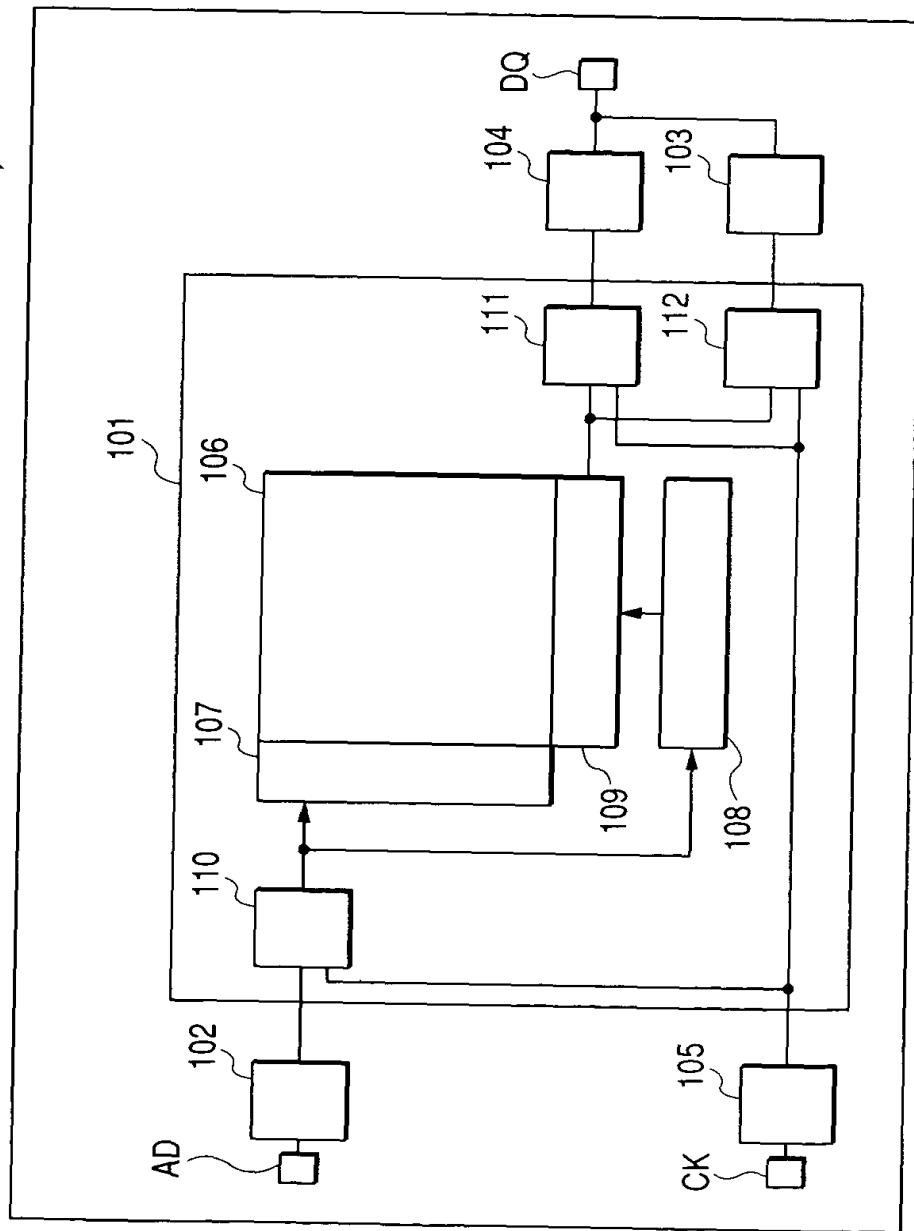


APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

1 / 30

FIG. 1

1a



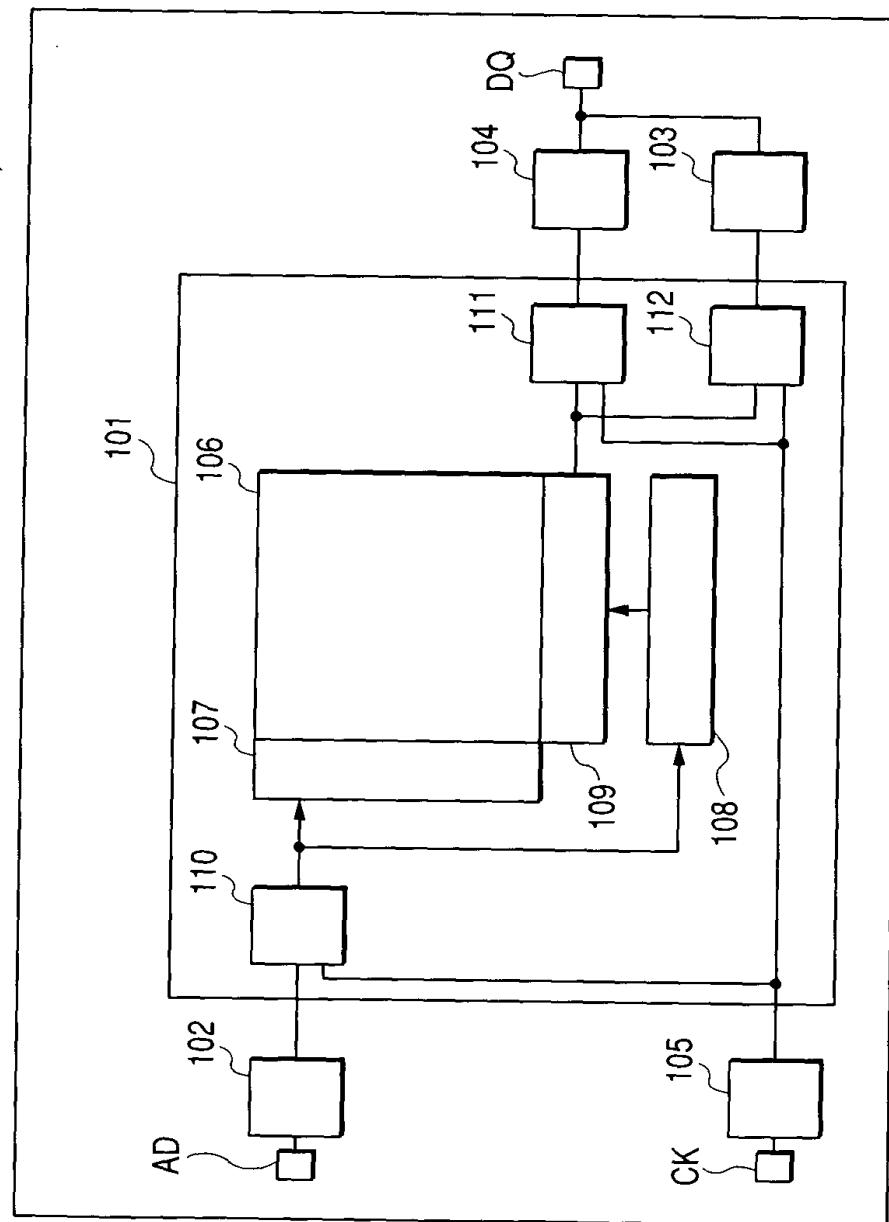
APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

2 / 30

FIG. 2

1b

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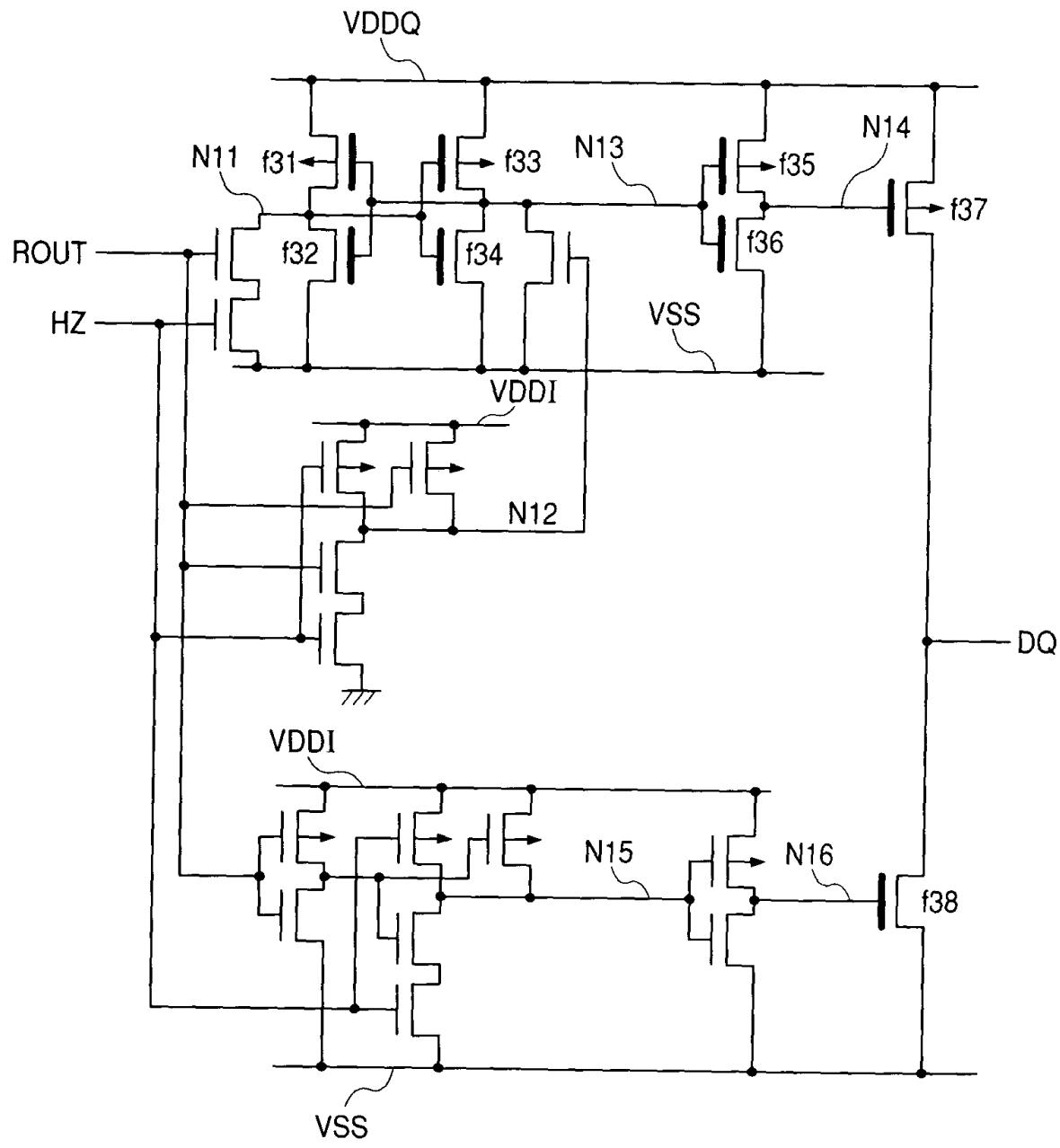


APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

3 / 30

*FIG. 3*

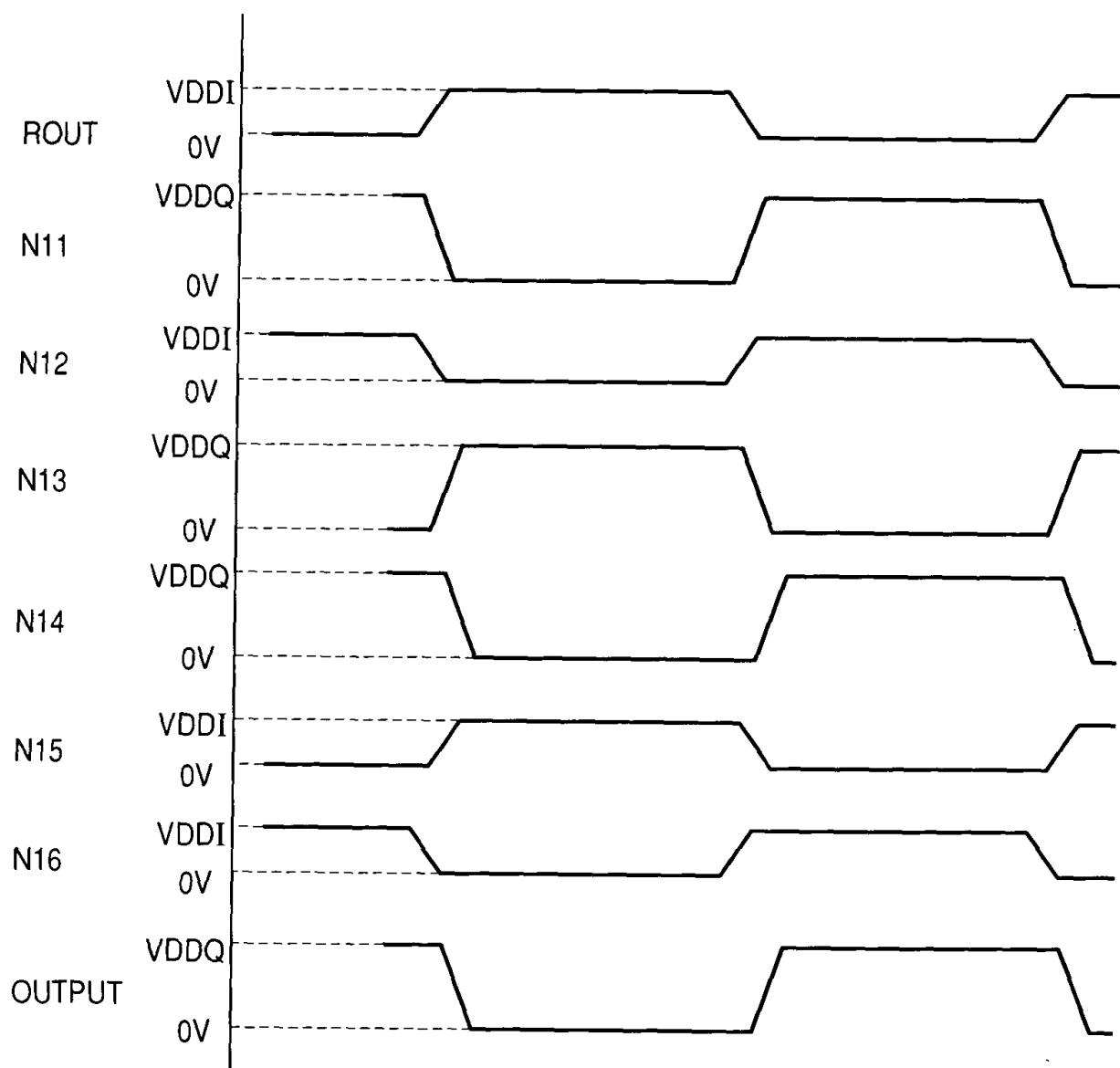
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4 / 30

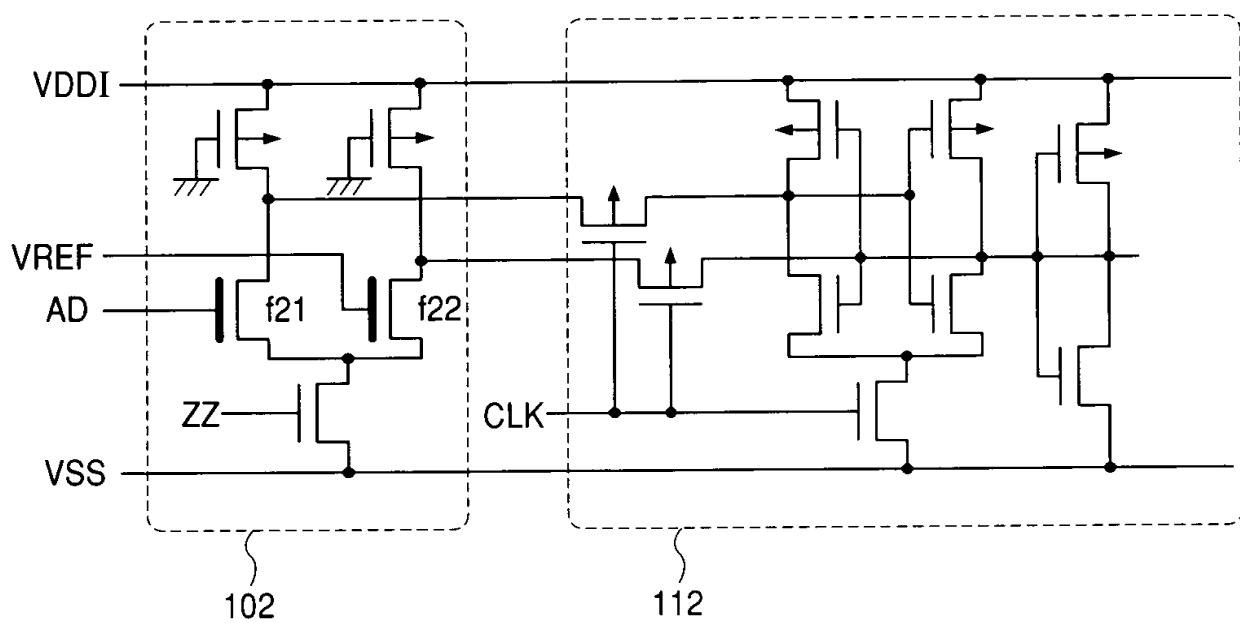
*FIG. 4*



APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

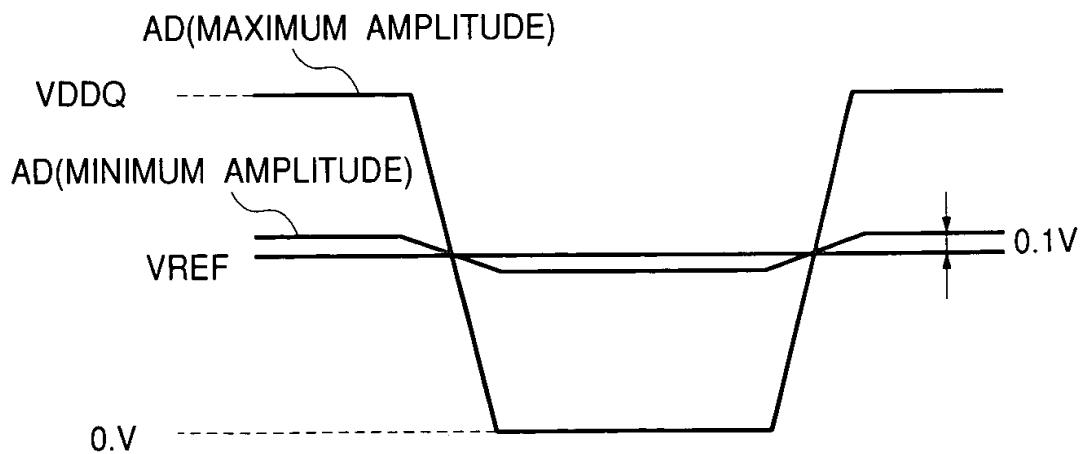
5 / 30

*FIG. 5*



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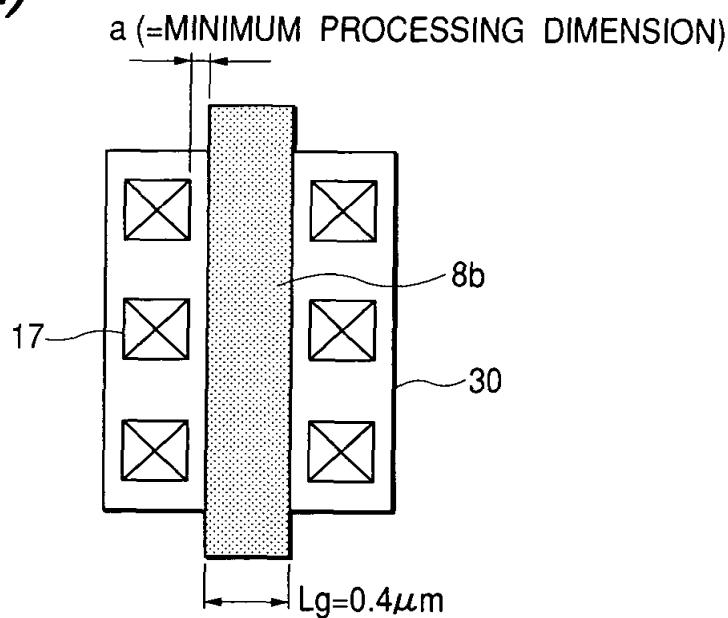
*FIG. 6*



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

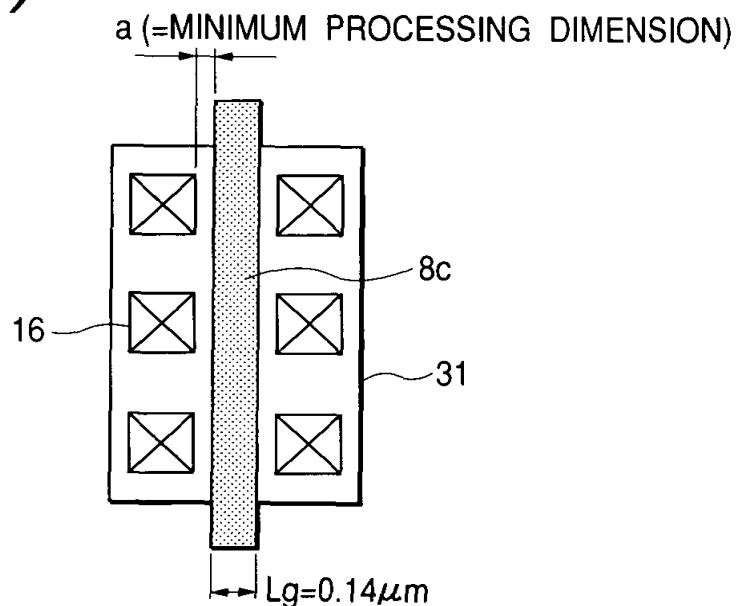
6 / 30

**FIG. 7(a)**



3.3V WITHSTANDING MOS TRANSISTOR

**FIG. 7(b)**

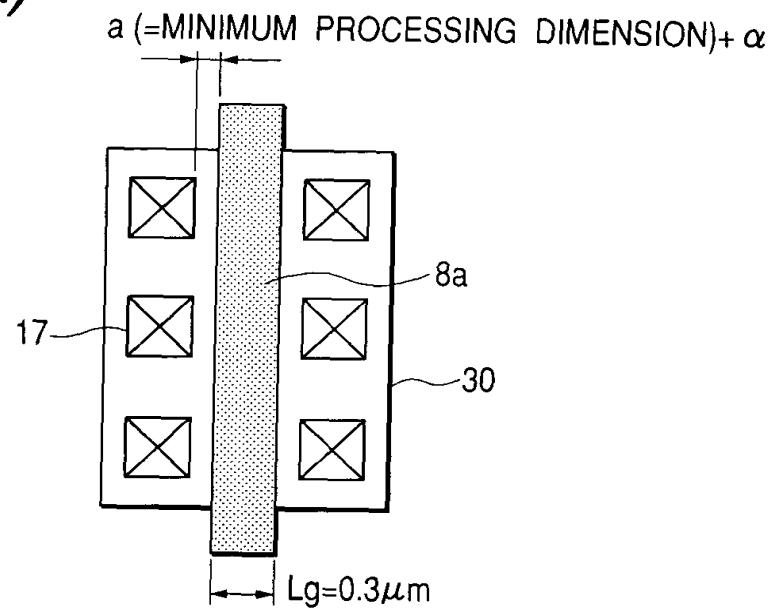


1.5V WITHSTANDING MOS TRANSISTOR

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

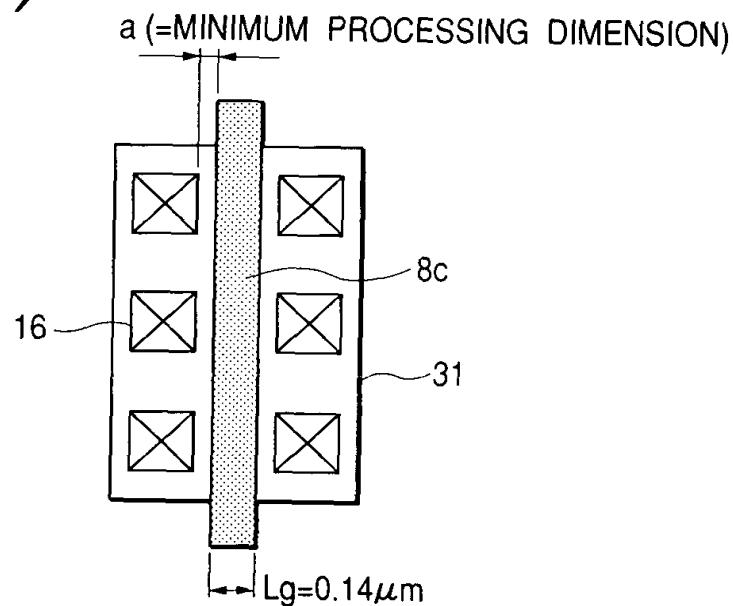
7 / 30

**FIG. 8(a)**



2.5V WITHSTANDING MOS TRANSISTOR

**FIG. 8(b)**



1.5V WITHSTANDING MOS TRANSISTOR

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

8 / 30

FIG. 9

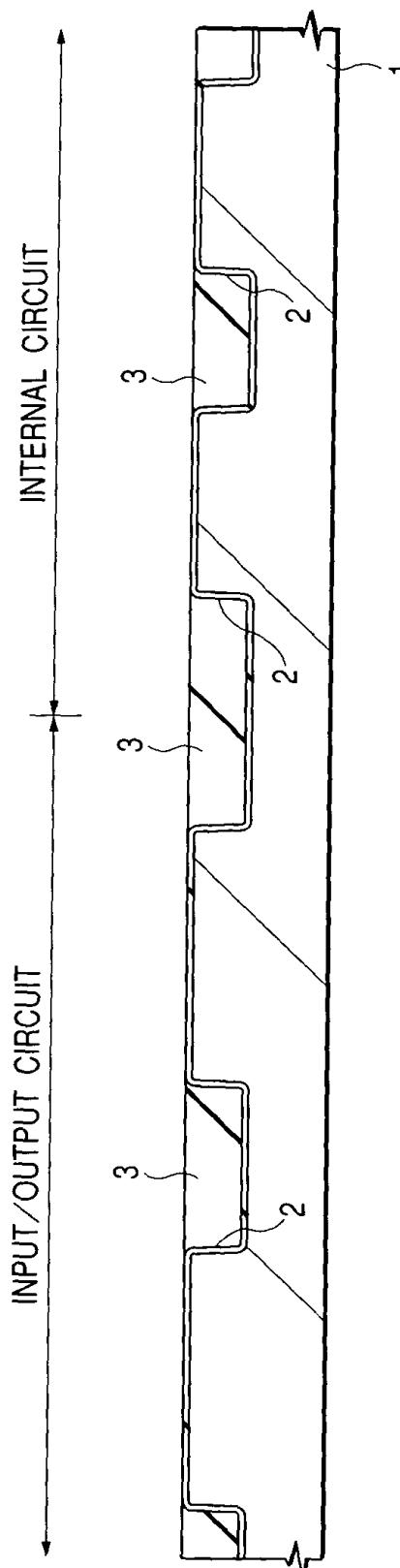
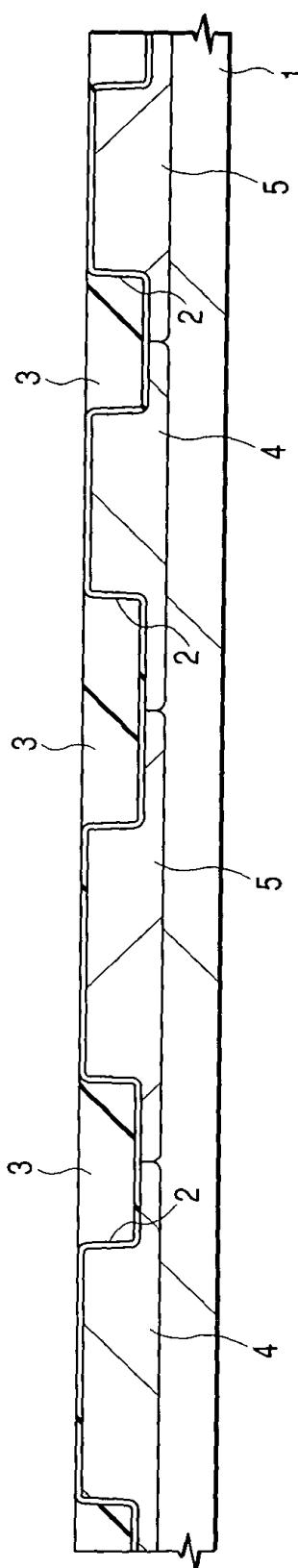


FIG. 10



APPROVED	O.G. FIG.
BY	CLASS / SUBCLAS
DRAFTSMAN	

9 / 30

FIG. 11(a)

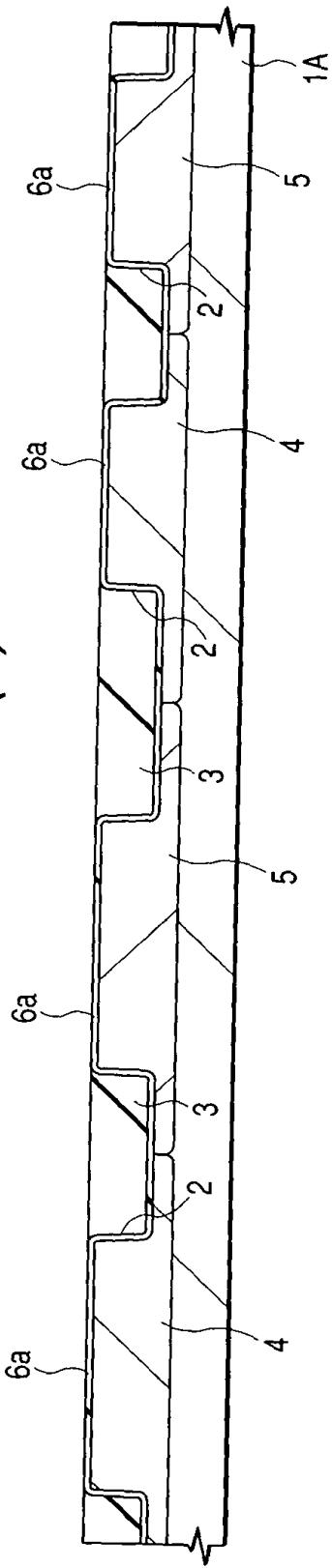
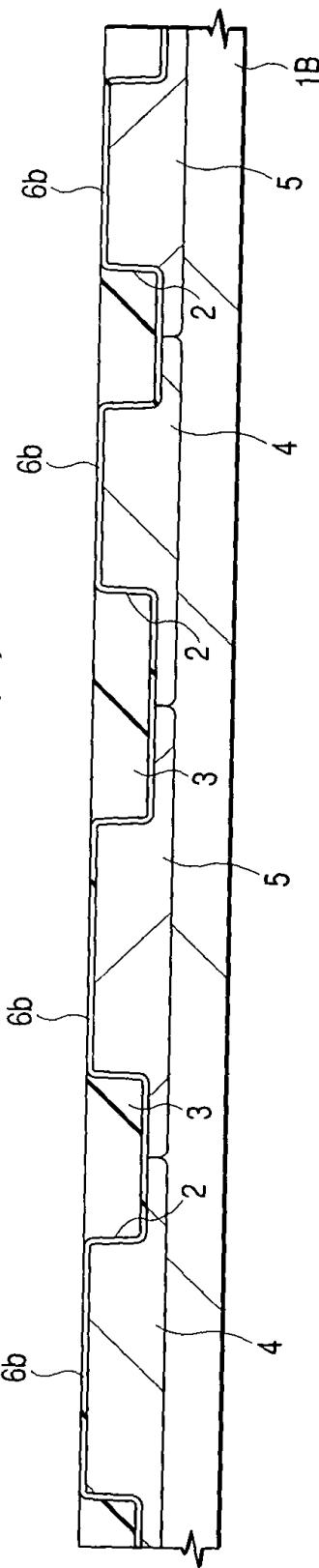


FIG. 11(b)



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

10 / 30

FIG. 12(a)

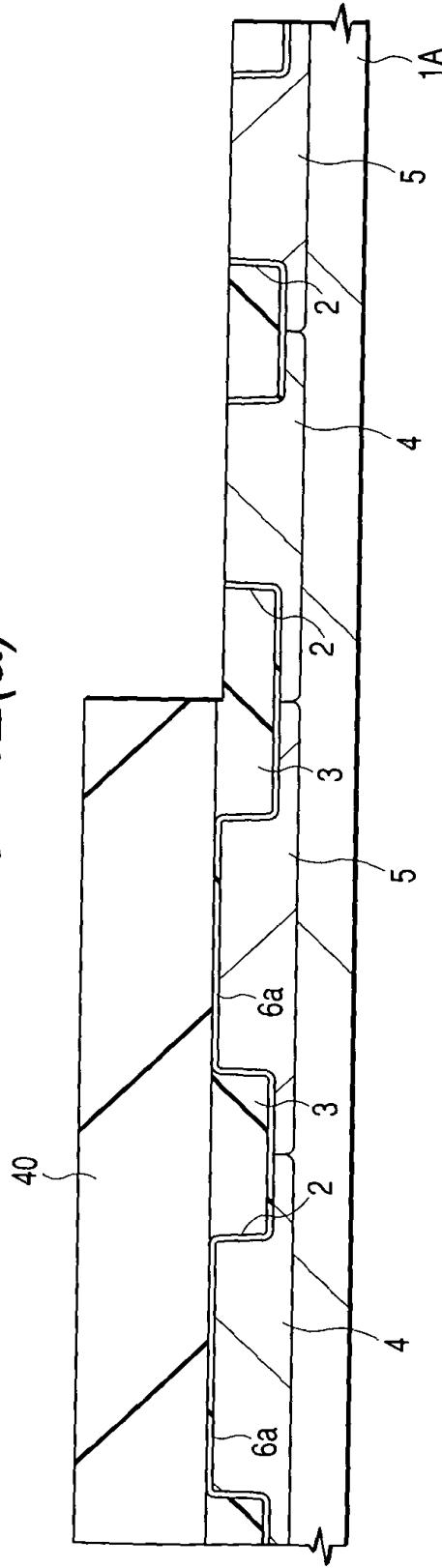
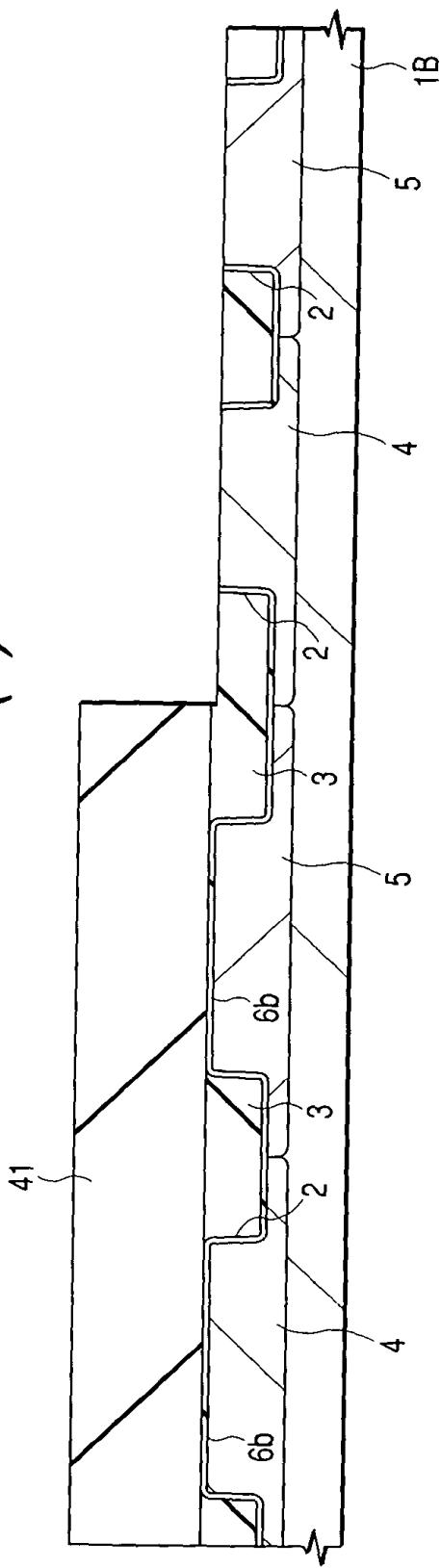


FIG. 12(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

11 / 30

FIG. 13(a)

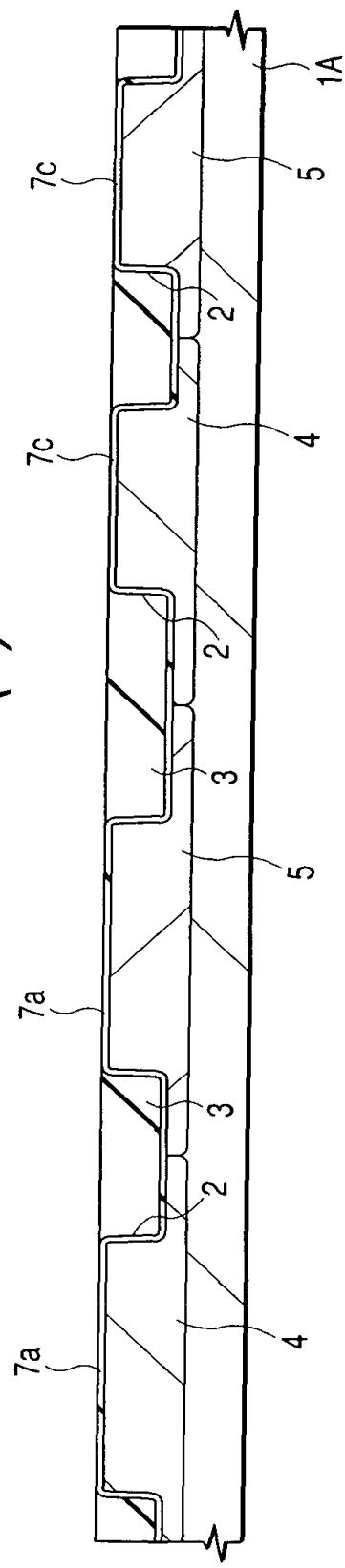
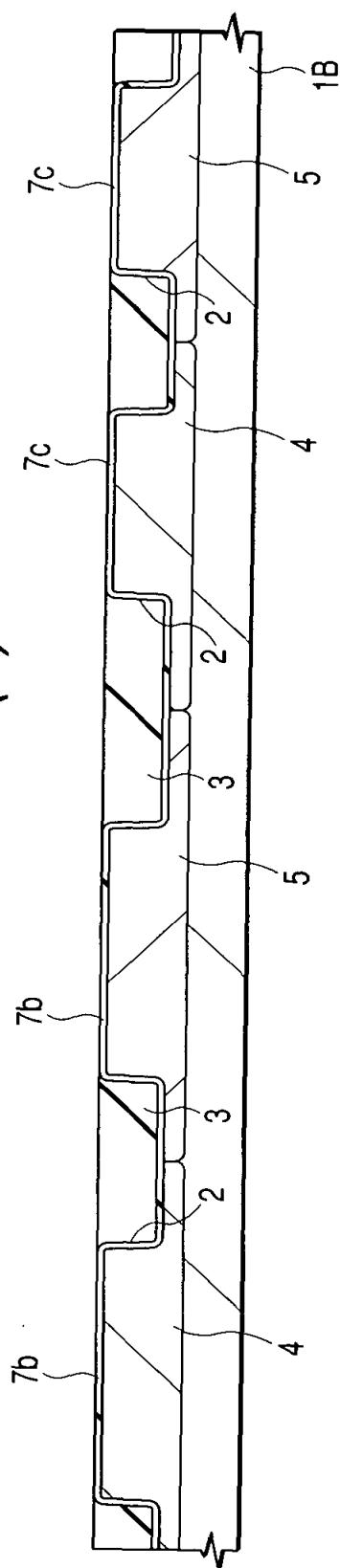


FIG. 13(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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12 / 30

FIG. 14(a)

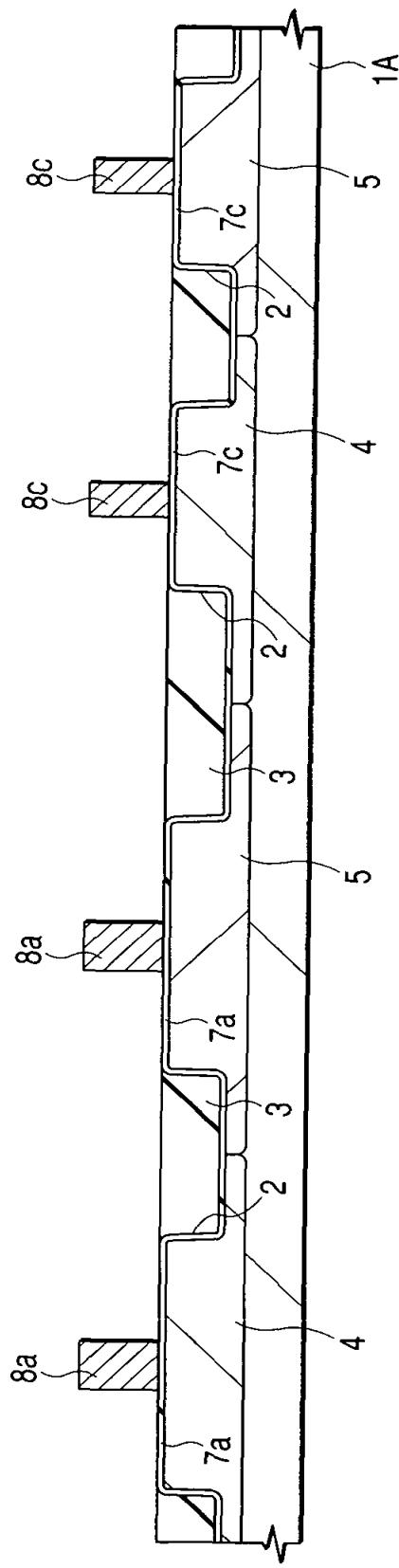
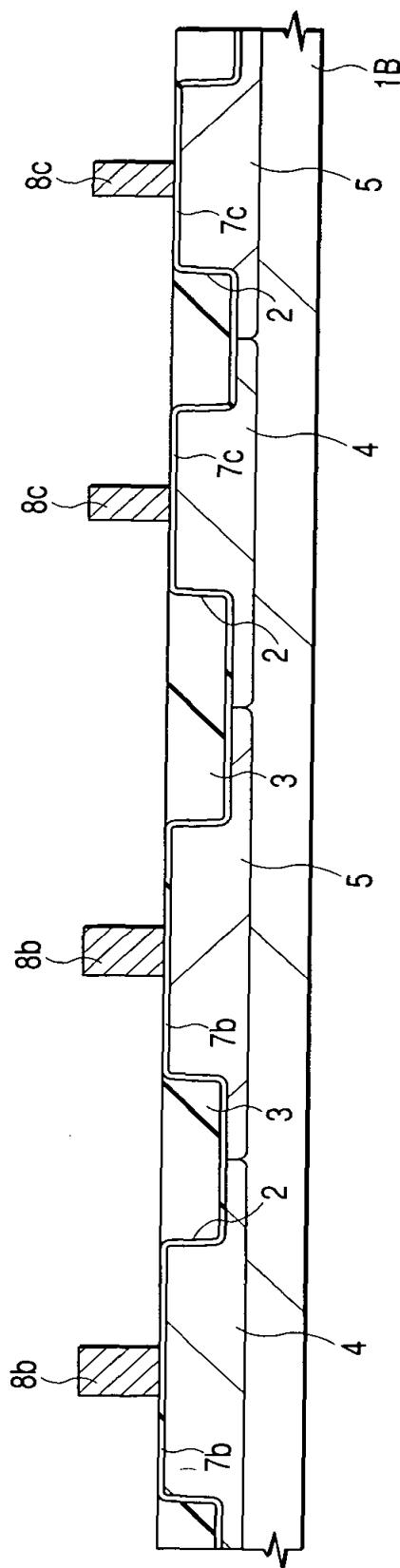


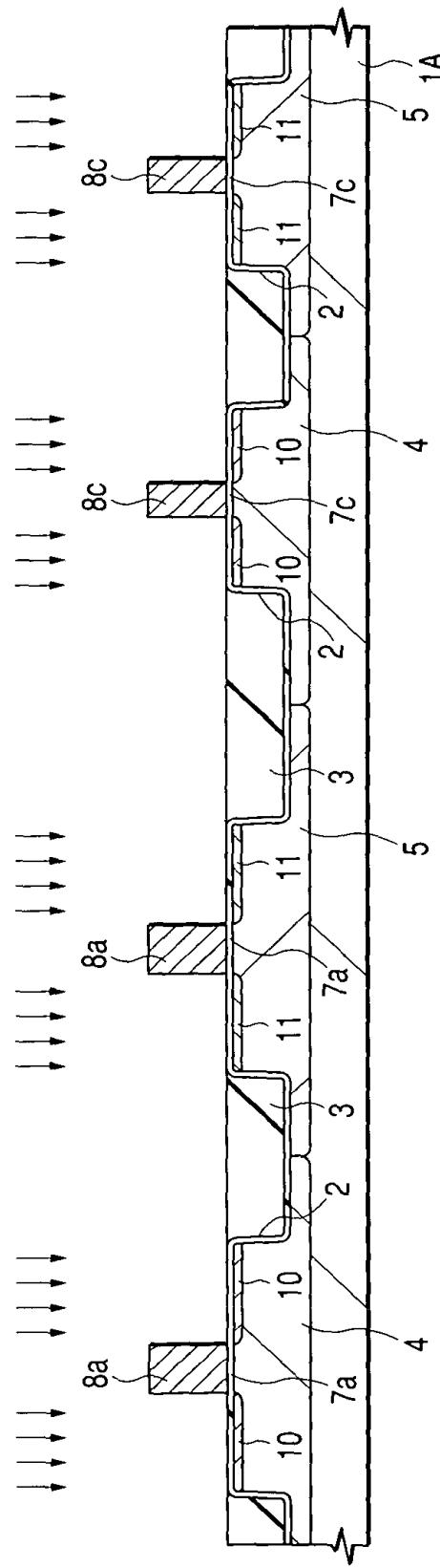
FIG. 14(b)



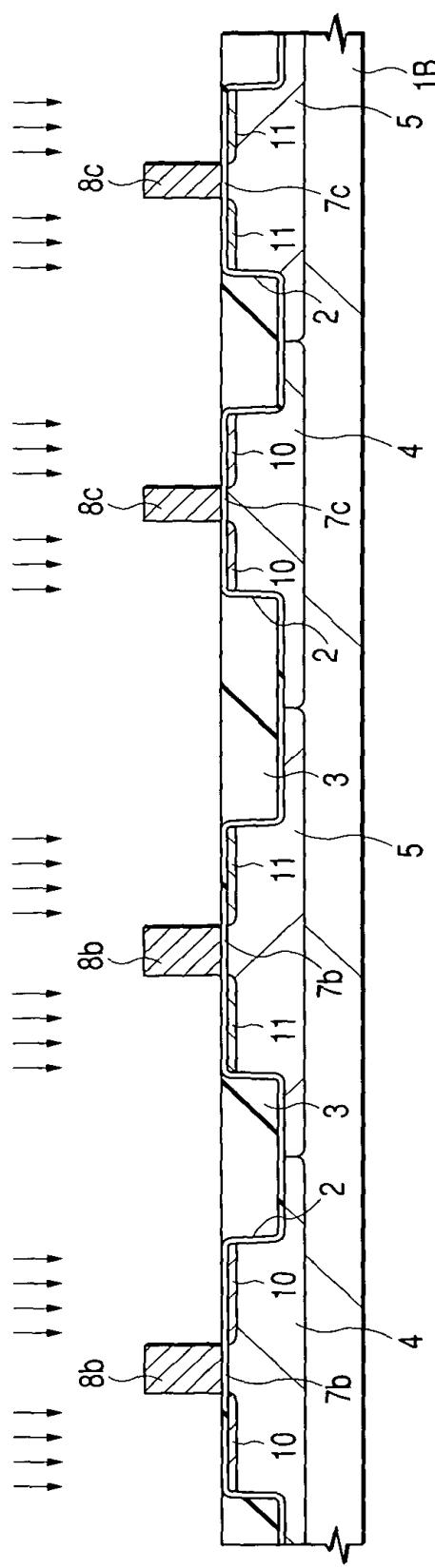
APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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13 / 30

*FIG. 15(a)*



*FIG. 15(b)*



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FIG. 16(a)

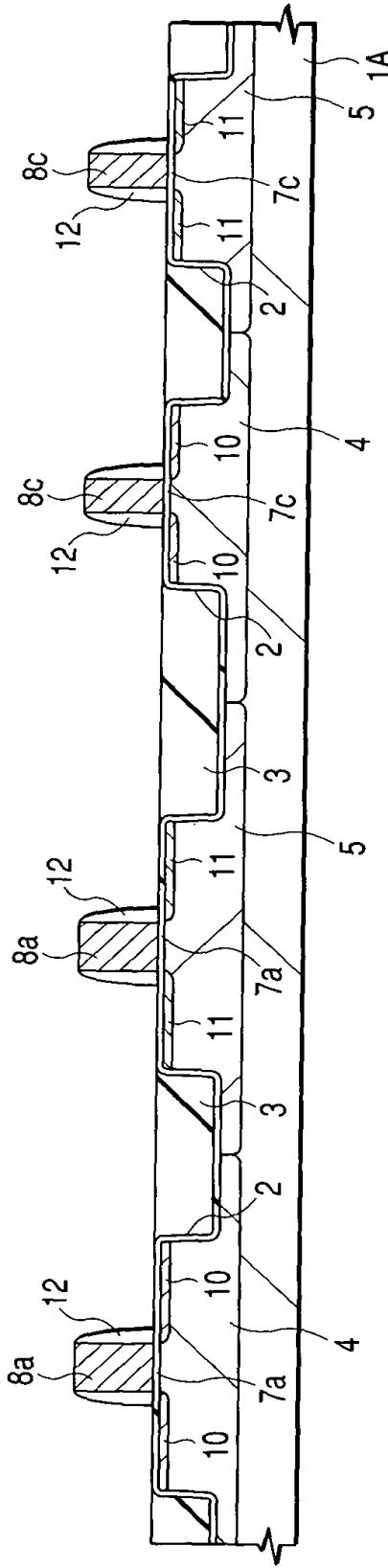


FIG. 16(b)

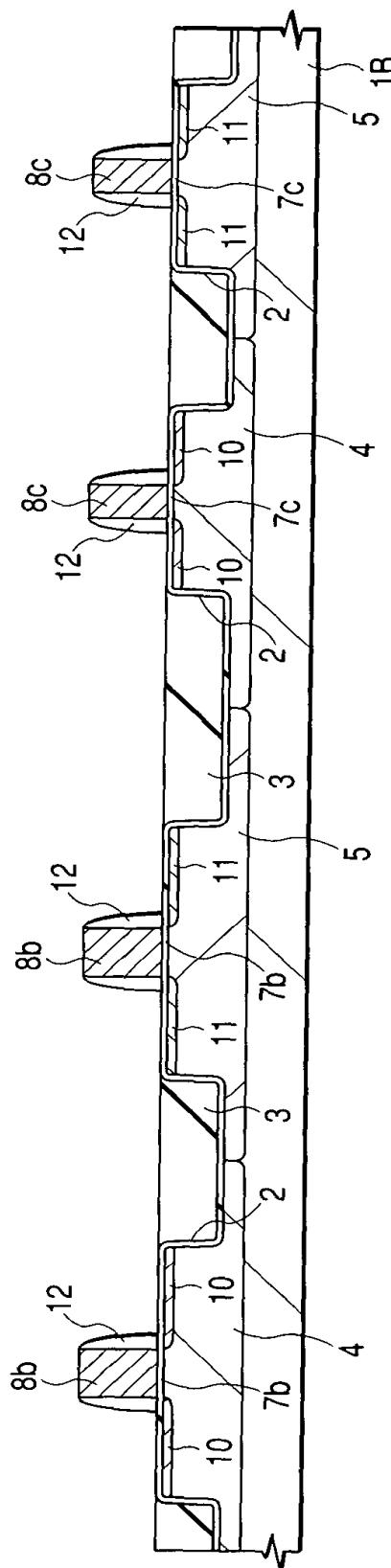


FIG. 17(a)

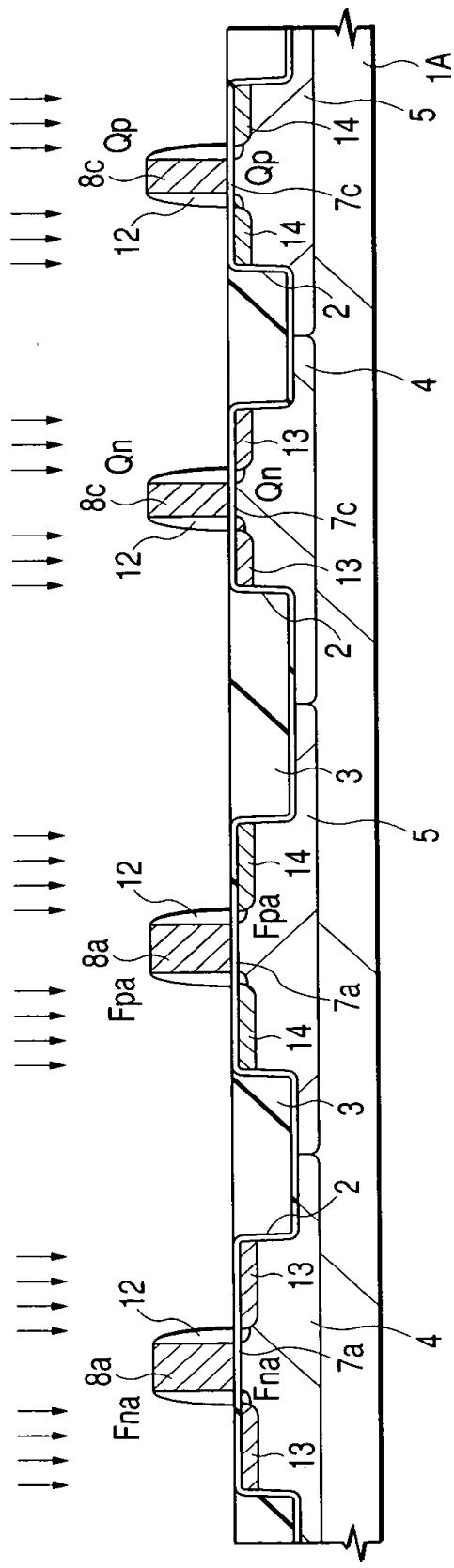
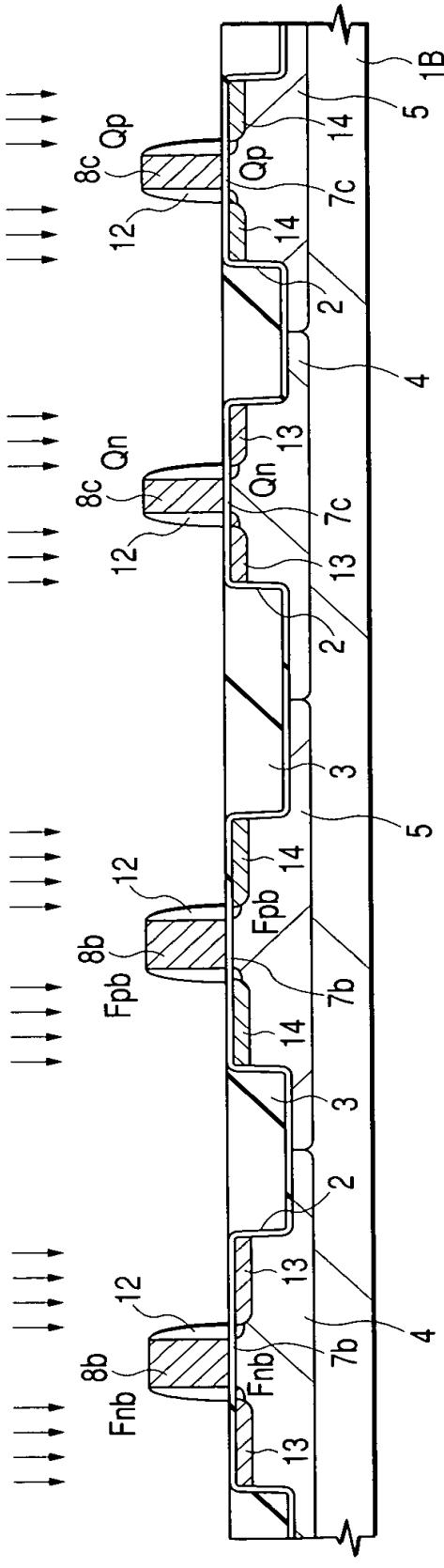


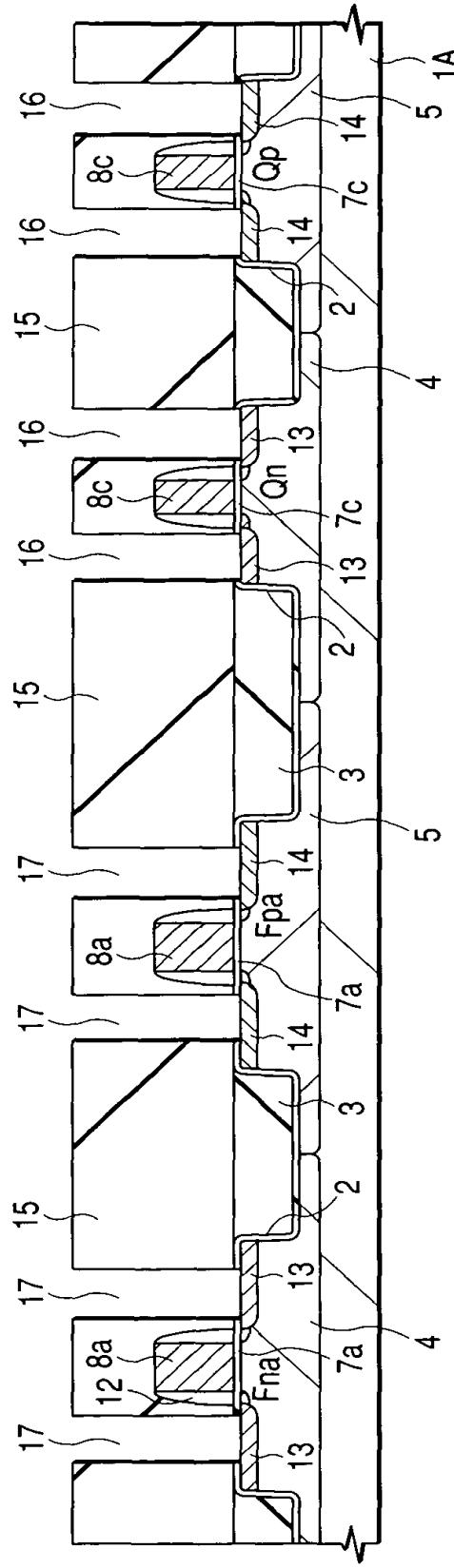
FIG. 17(b)



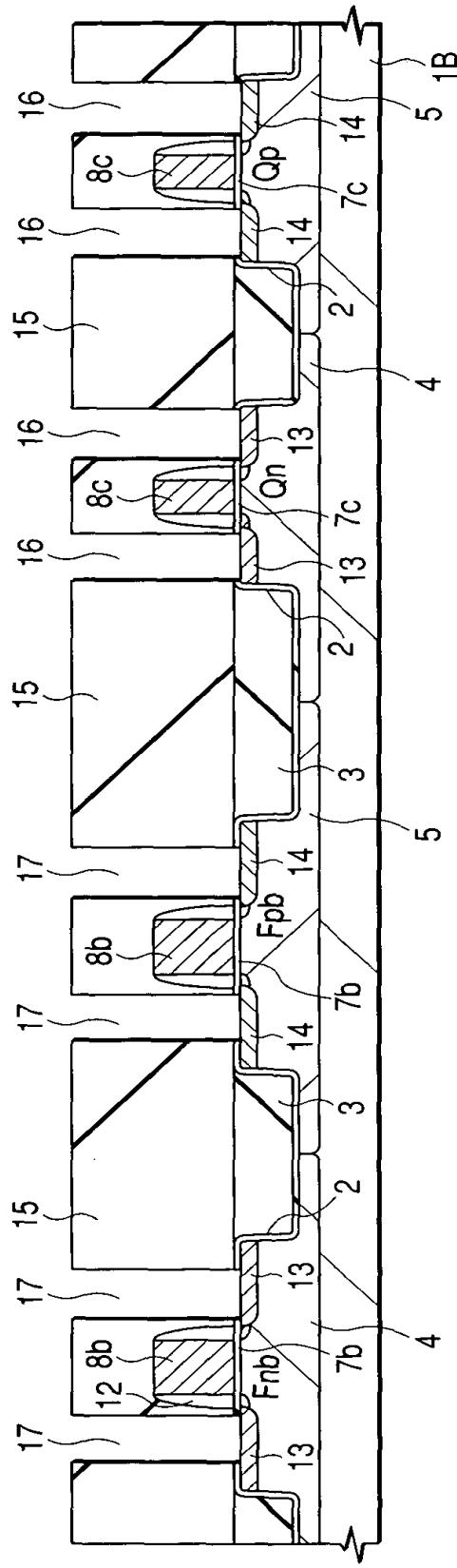
APPROVED BY	O.G. FIG.
	CLASS SUBCLASS
DRAFTSMAN	

16 / 30

**FIG. 18(a)**



**FIG. 18(b)**



16 0502 T 6002 2000 T

**FIG. 19**

a (=MINIMUM PROCESSING DIMENSION)

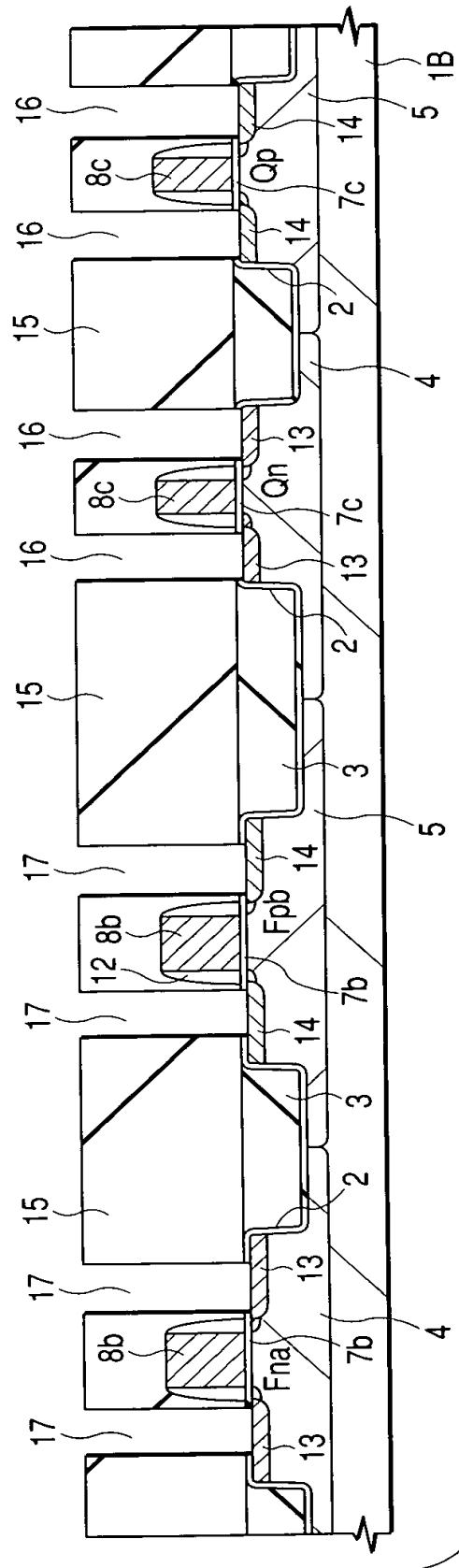
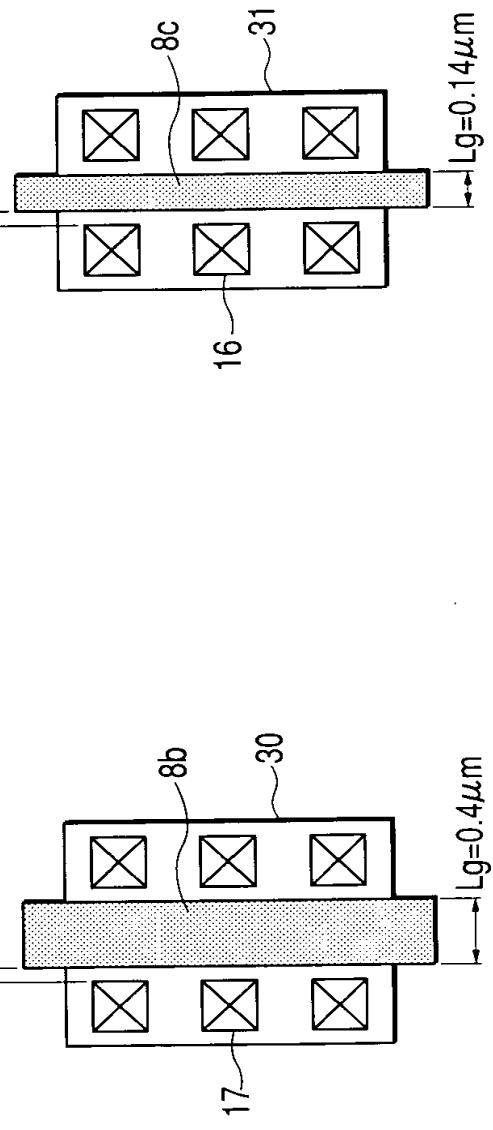
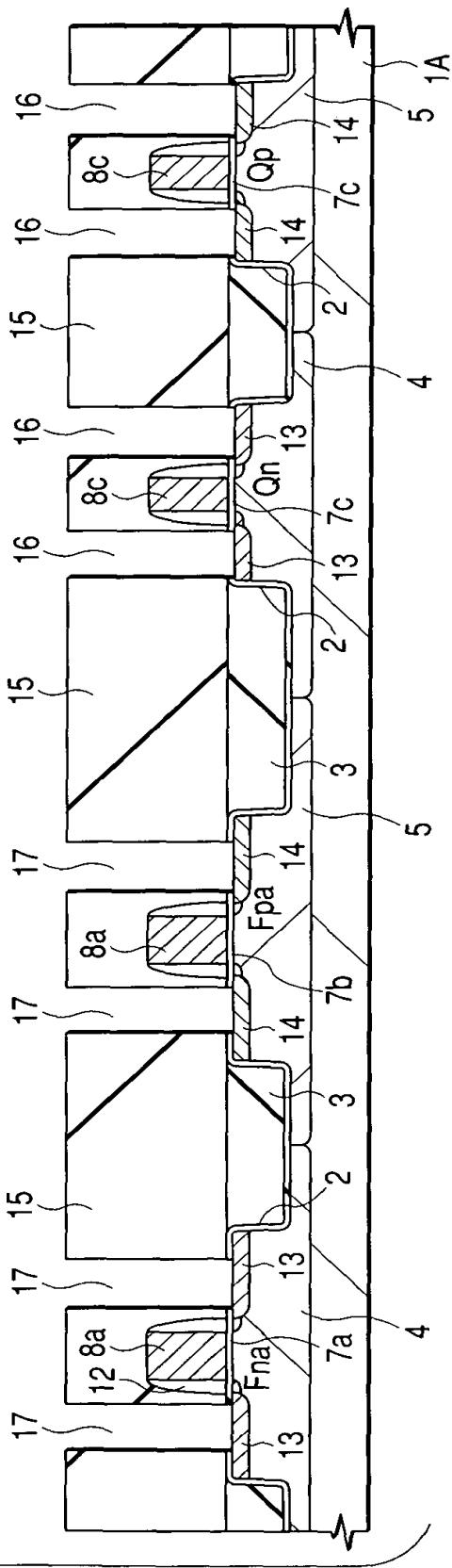
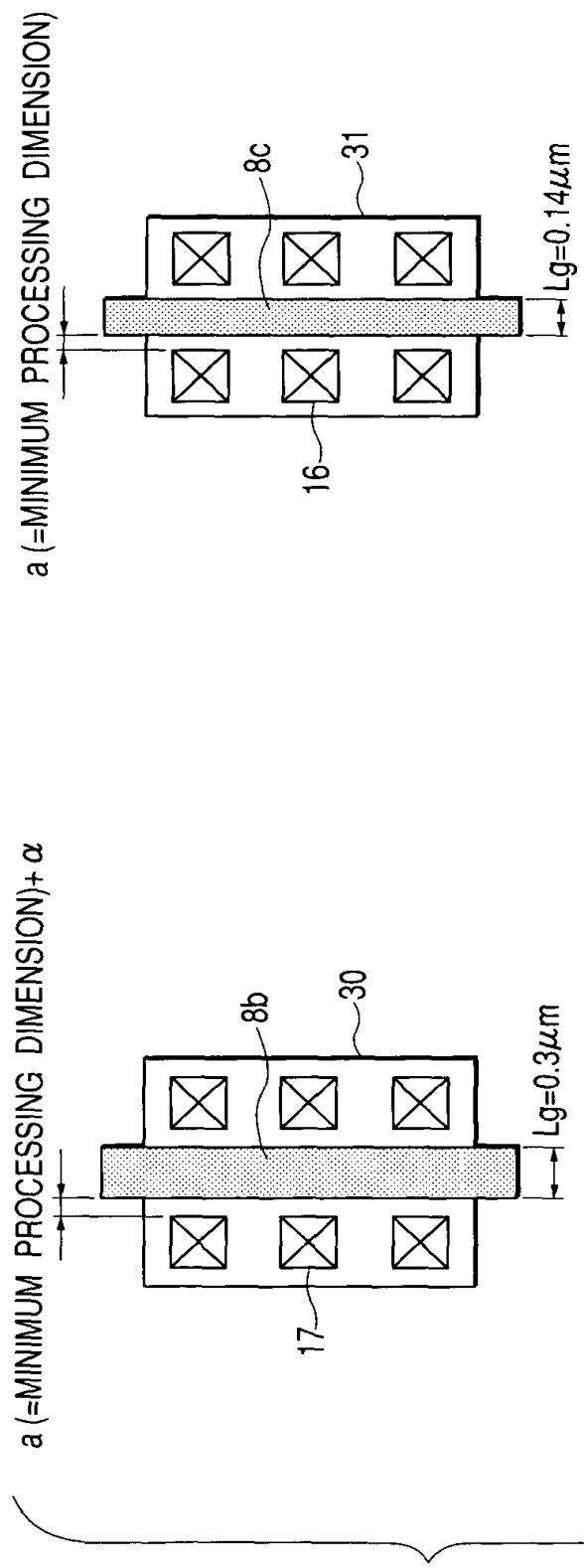


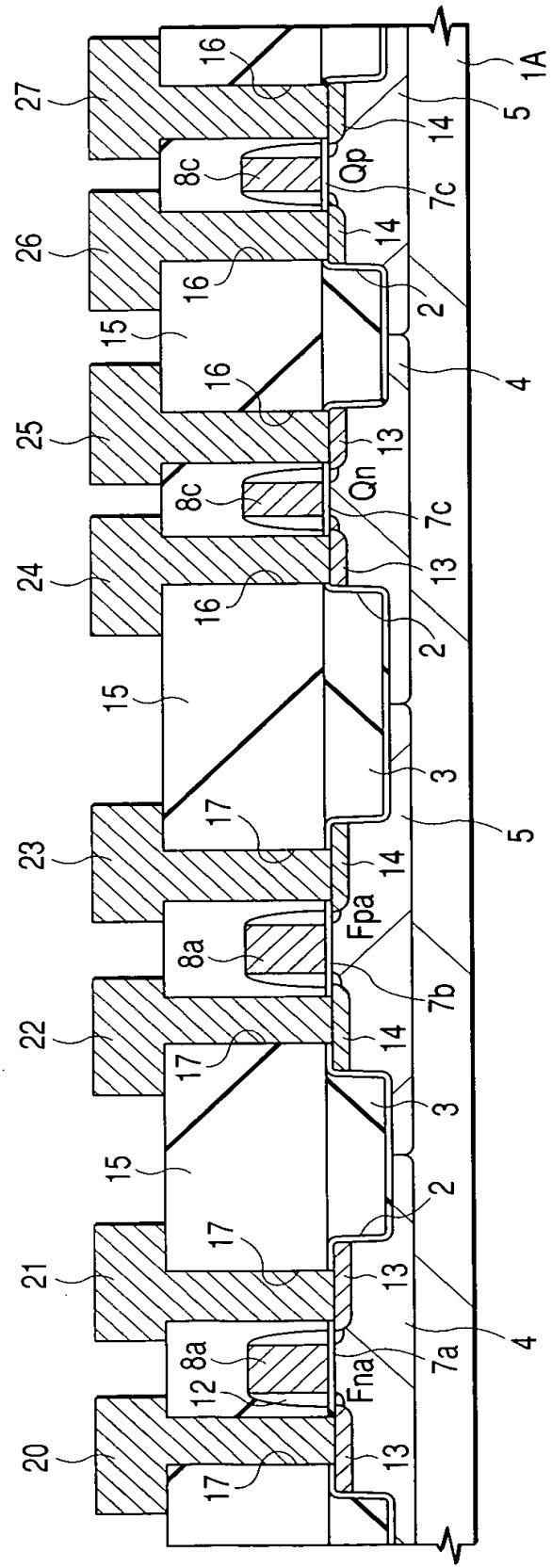
FIG. 20



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

19 / 30

FIG. 21



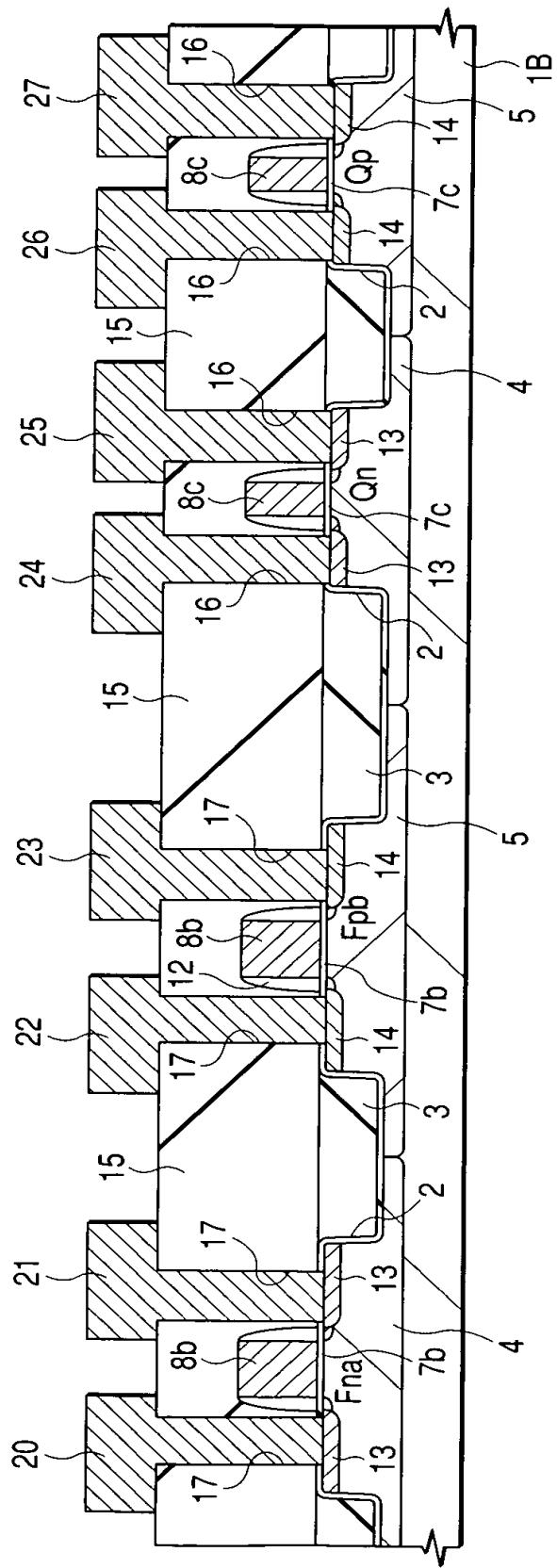
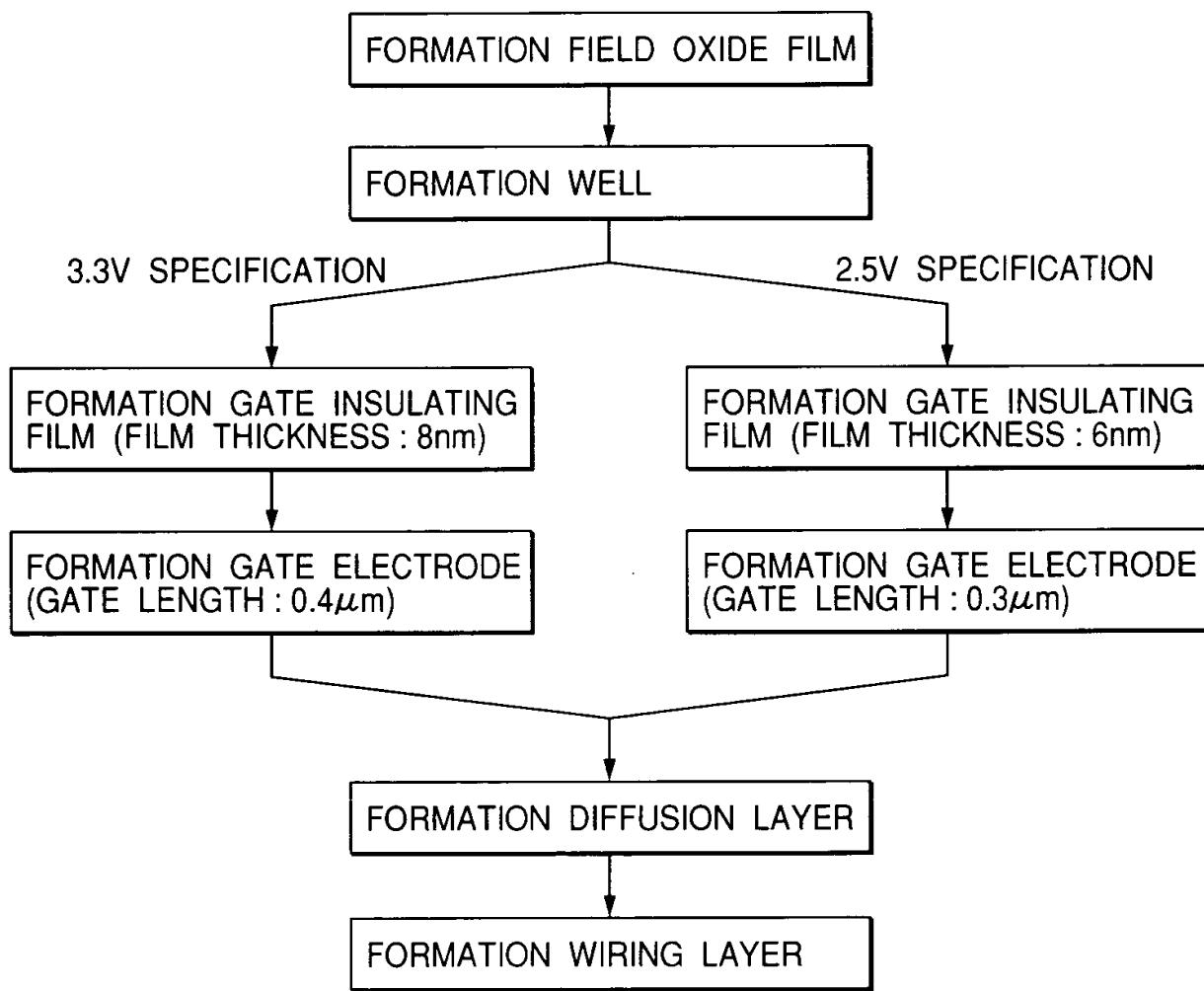


FIG. 22

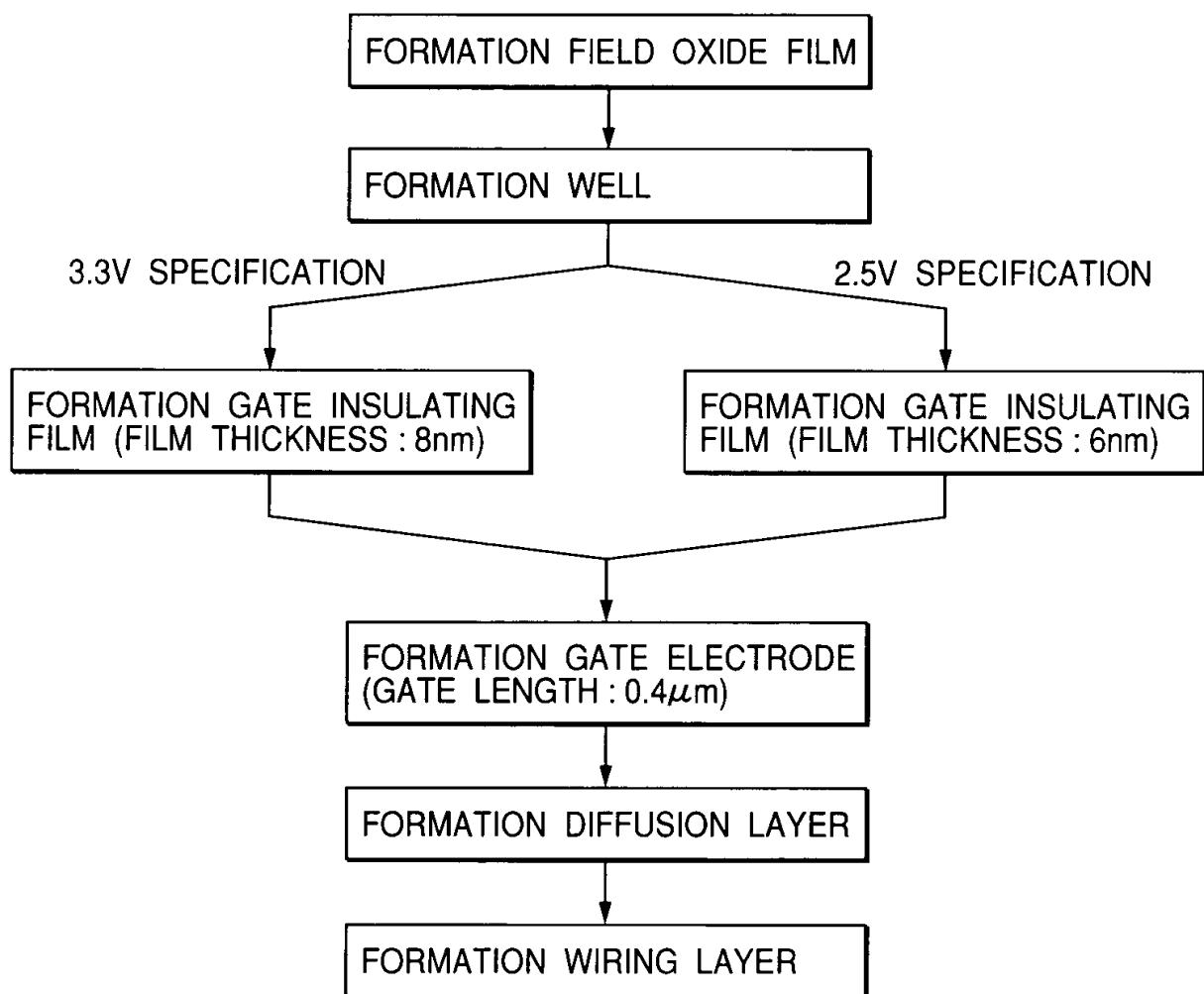
**FIG. 23**



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

22 / 30

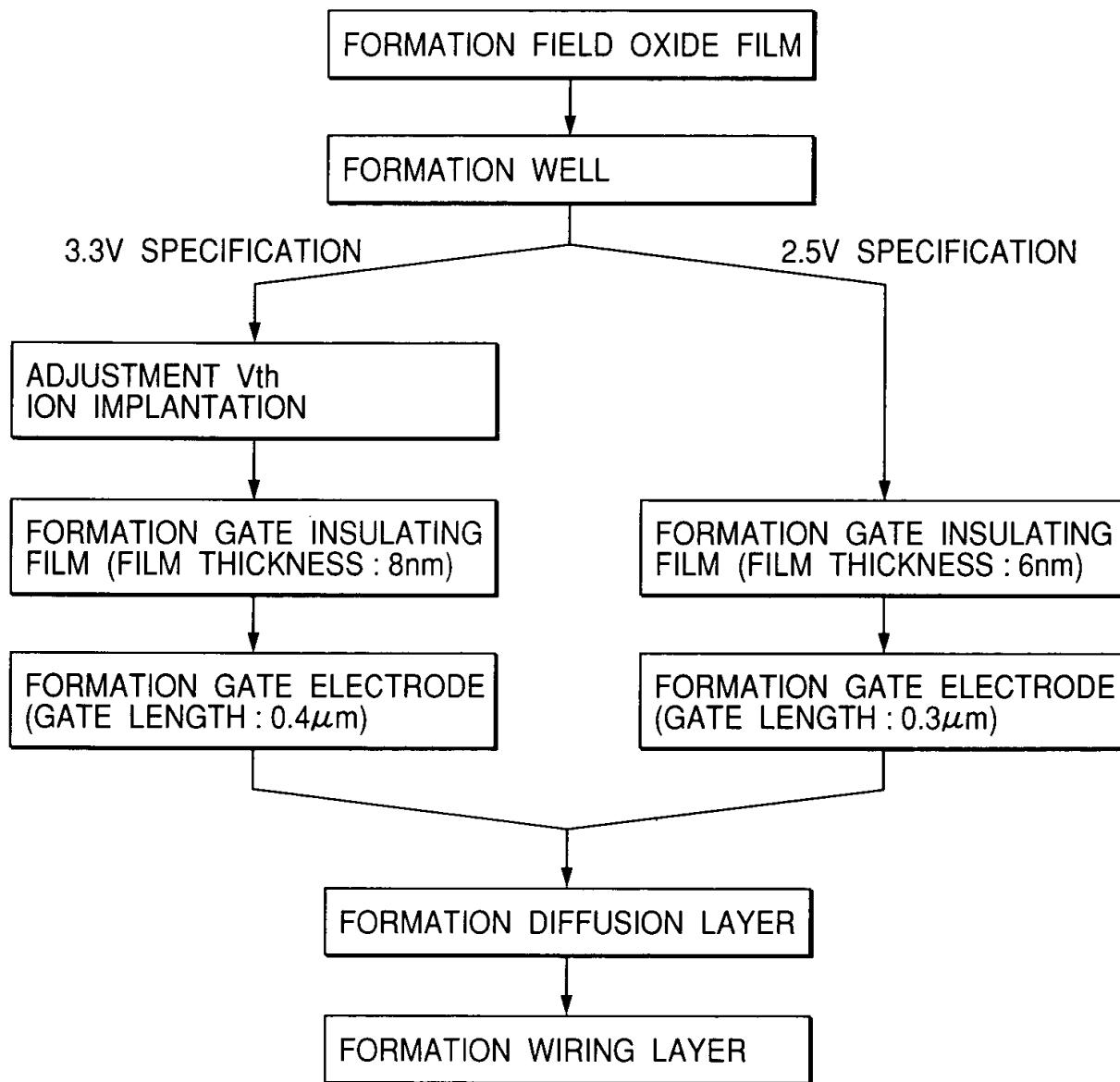
## FIG. 24



APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS

## FIG. 25

THE JAPANESE INDUSTRIAL STANDARDS

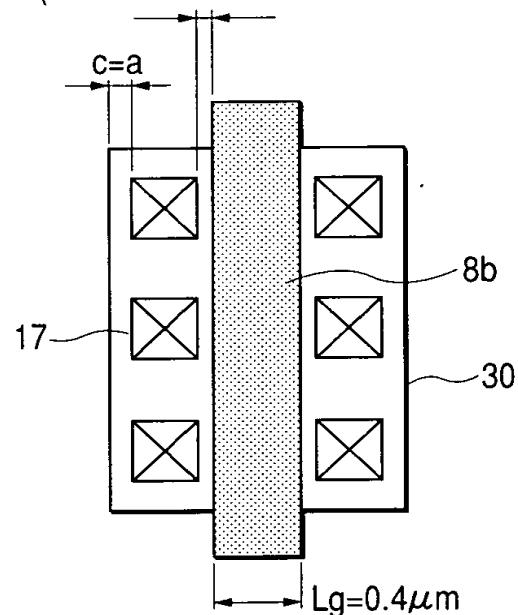


APPROVED BY	O.G. FIG.
	CLASS
DRAFTSMAN	SUBCLASS

24 / 30

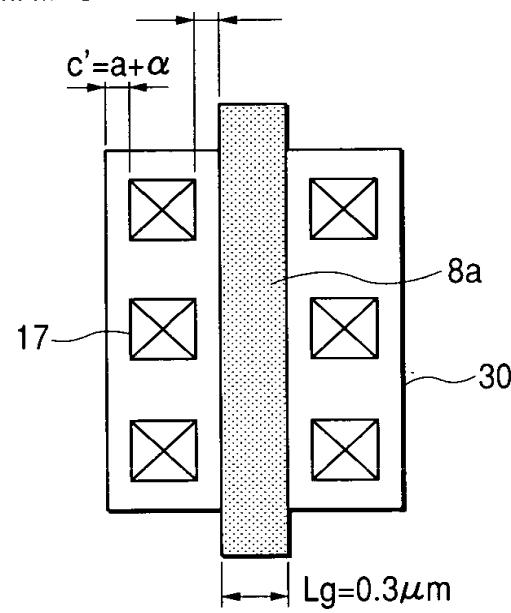
**FIG. 26**

a (=MINIMUM PROCESSING DIMENSION)



3.3V WITHSTANDING MOS TRANSISTOR

a (=MINIMUM PROCESSING DIMENSION)



2.5V WITHSTANDING MOS TRANSISTOR

APPROVED BY	O.G. FIG. CLASS	SUBCLASS
DRAFTSMAN		

25 / 30

## FIG. 27

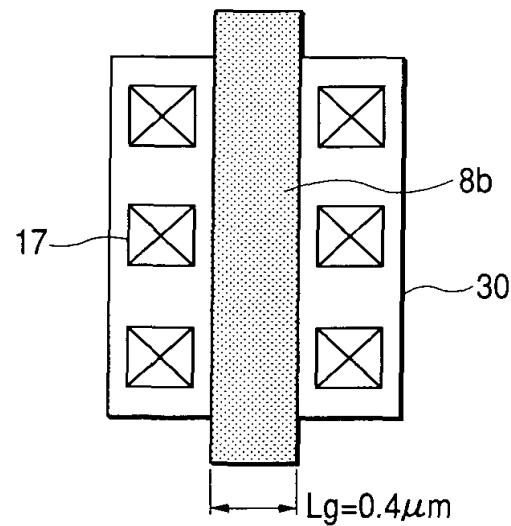
SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	1.5V	0V	VDDQ	1.5V

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

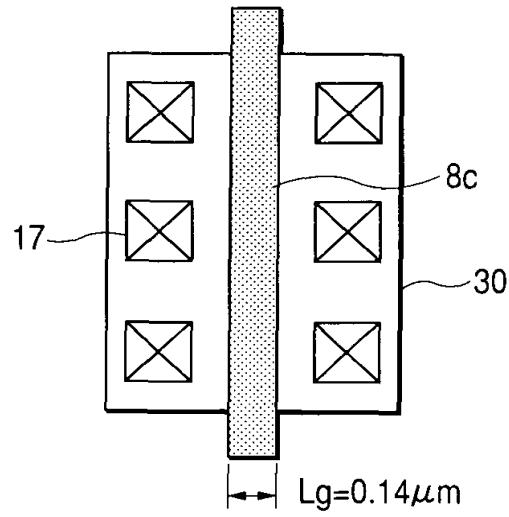
26 / 30

*FIG. 28*

PATENT DRAWINGS  
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3.3V WITHSTANDING MOS TRANSISTOR



2.5V WITHSTANDING MOS TRANSISTOR

APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	O.G. FIG. SUBCLASS
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27 / 30

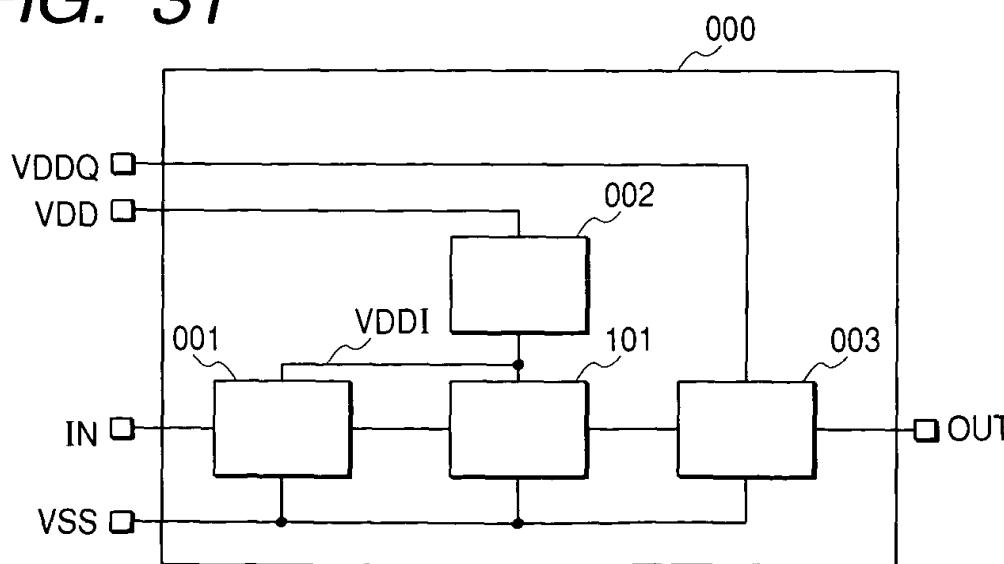
**FIG. 29**

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	2.5V	0V	VDDQ	1.5V

**FIG. 30**

	GATE INSULATING FILM THICKNESS	MINIMUM PROCESSING GATE LENGTH
	TOX	Lg
3.3V WITHSTANDING MOS	8nm	0.4μm
2.5V WITHSTANDING MOS	6nm	0.3μm
1.5V WITHSTANDING MOS	3nm	0.14μm

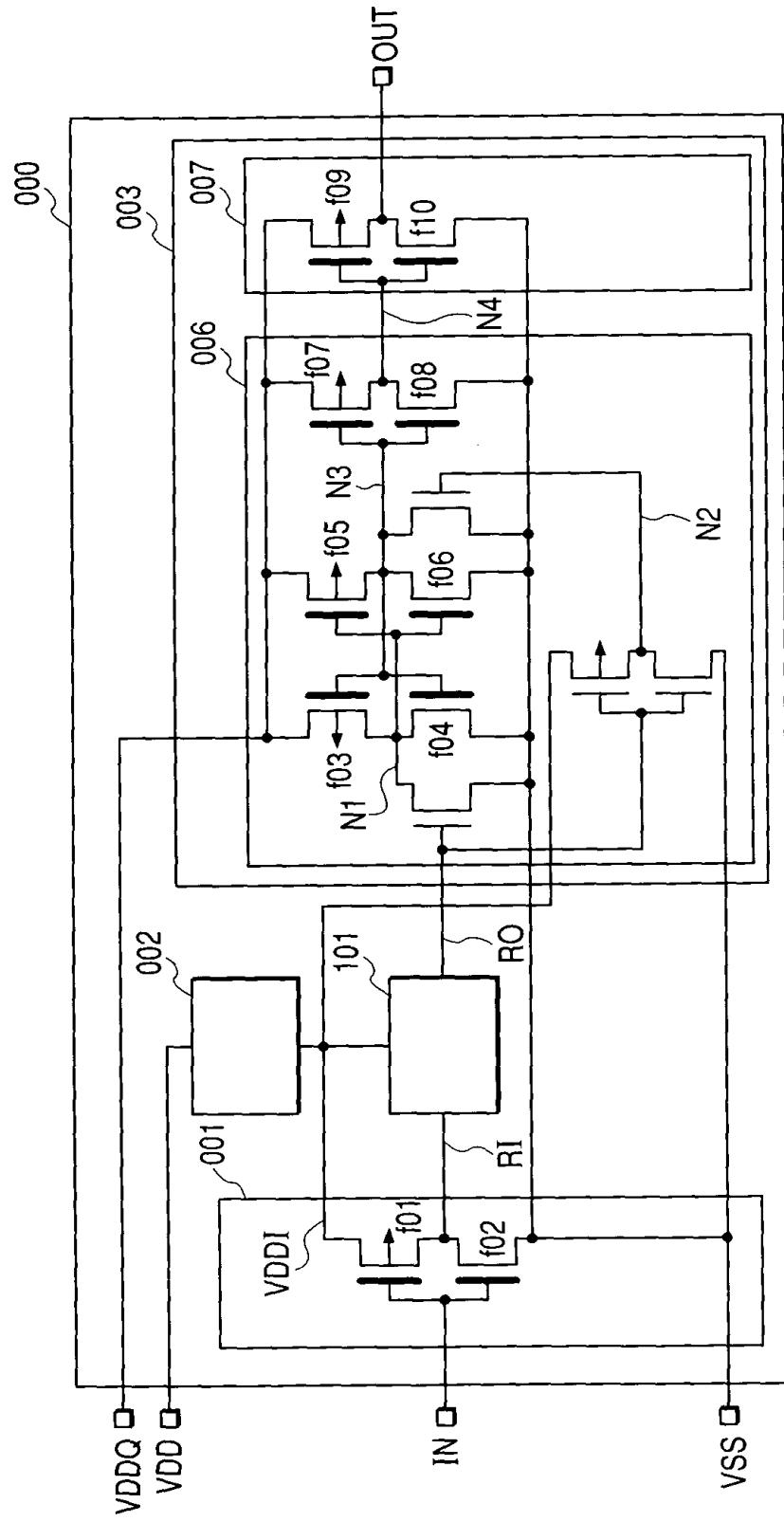
**FIG. 31**



APPROVED	O.G. FIG.
BY	CLASS
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28 / 30

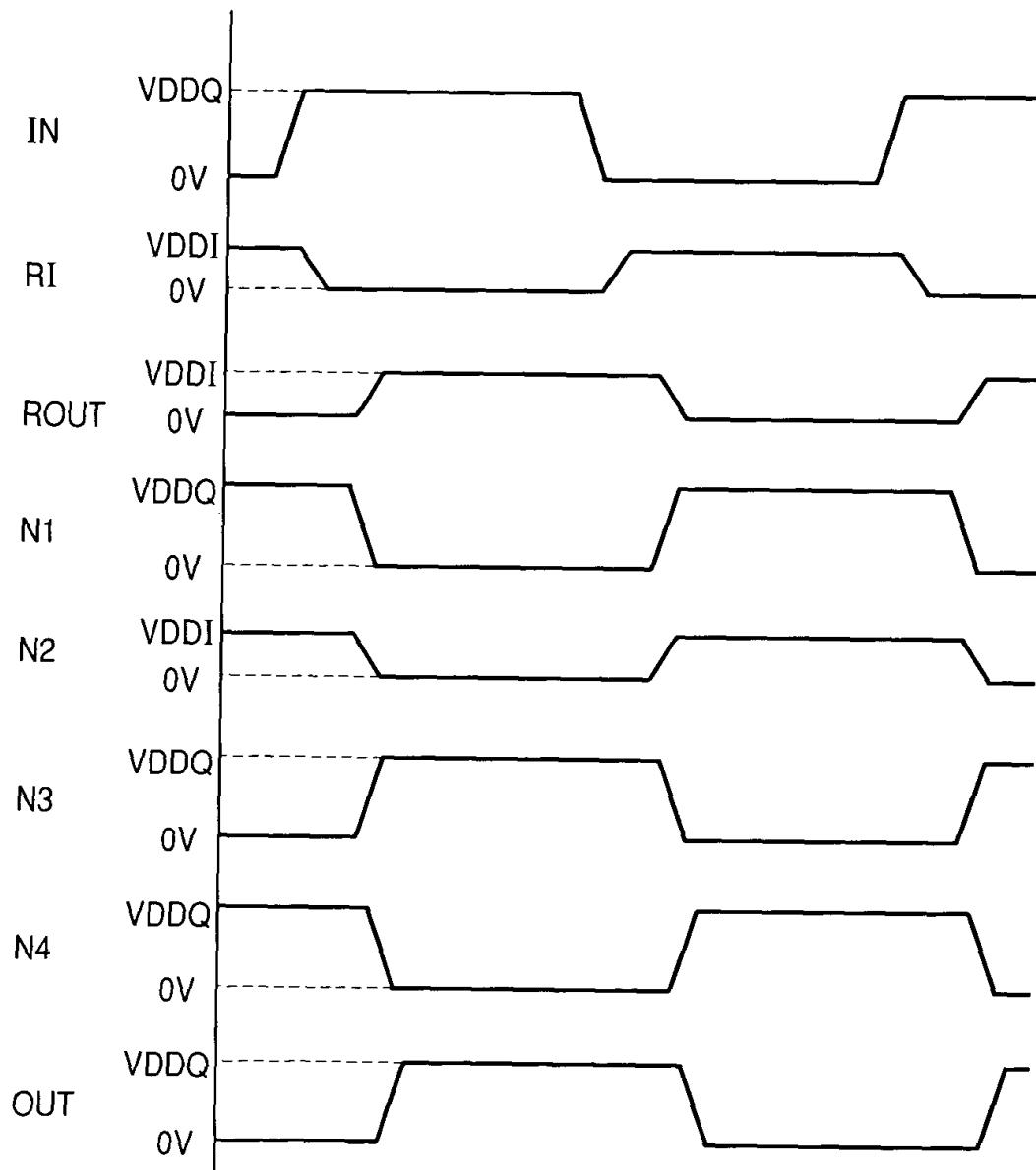
FIG. 32



APPROVED BY	O.G. FIG.
DRAFTSMAN	CLASS
	SUBCLASS

29 / 30

*FIG. 33*



APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

30 / 30

FIG. 34

